CLAIMS

1. A method for processing tasks in a data processing system including a microprocessor and an instruction cache wherein tasks of different types are defined in the system, each task type having code associated therewith, the tasks being processed in order by loading the associated code into the instruction cache for execution on the microprocessor, the method comprising the step of placing the tasks of at least one task type into a batch such that the tasks in a batch are processed before processing the next ordered task.

2. A method as claimed in claim 1 wherein the code associated with at least one type of task fits within the instruction cache, the method comprises the further steps of: processing such a task by loading the associated code into the instruction cache and executing the code on the microprocessor, and on a determination that there is a further task of like type in the batch, executing the loaded code to process the further task.

3. A method as claimed in claim 1 wherein the code associated with at least one type of task is not capable of being loaded as a whole into the instruction cache, the code being logically divided at one or more break points into two or more portions, and wherein during processing of such a task, the method comprises the further steps of responding to a break point defined within a first portion of the code to schedule a further task for future execution of a second portion of the code.

4. A method as claimed in claim 3 wherein the further scheduled task is placed in a batch of like tasks.

5. A method as claimed in claim 3 wherein each of portions of code defines an atomic operation.

6. A method as claimed in claim 1, wherein a task is placed in a batch at the time the task is scheduled.

7. A method as claimed in claim 1 wherein the tasks are managed as a queue.

8. A computer program product comprising a computer usable medium having computer readable program code means embodied in the medium for processing tasks in a data processing system, the data processing system including a microprocessor and an instruction cache and wherein tasks of different types are defined in the system, each task type having code associated therewith, the tasks being processed in order by executing the associated code on the microprocessor, the program code means comprising code means for scheduling tasks of like type into a batch such that tasks in a batch are processed before processing the next ordered task.

9. Data processing apparatus comprising a microprocessor and an instruction cache wherein tasks of different types are defined in the system, each task type having code associated therewith, the apparatus including:

means for processing the tasks in order by loading the associated code into the instruction cache for execution on the microprocessor; and

means for scheduling tasks of like type into a batch, wherein the means for processing the tasks is operable to process the tasks in a batch before processing the next ordered task.

10. Data processing apparatus as claimed in claim 9 wherein the microprocessor and i-cache are embodied on a single chip.

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